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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/685,272	10/09/2000	Eric M. Dowling	SEARCHP.008DV1	4446

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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	10

DATE MAILED: 01/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/685,272	DOWLING, ERIC M.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- Th MAILING DATE of this communication app ars on th cover sheet with th correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-29,33-74 and 77-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *79* is/are allowed.

6)☒ Claim(s) *24-29,33-74,77 and 78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 11/12/2003.

As indicated in Applicant's response, claims 24, 33, 42, 51, 60, and 69 have been amended and claims 75-76 canceled. Claims 24-29, 33-74, 77-79 are pending in the office action.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 33-41 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 33 recites of a method of supplying software; and a method is required to be within the ambit of a tangible, practical and useful process. In that regard, the claimed invention is not patentable subject matter.

Claims 33-41 fail to recite method steps in the technological or useful arts, instead, recite nothing more than "supplying" software modules. Further definition of what is contained within the modules, as recited in both the independent and/or dependent claims, fails to rectify the problem of the independent claim, since nothing recites actual execution of the supplied modules. Absent execution, the modules have no useful result.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130 (b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 24-29, 42-74, 77-78 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,163,836 (hereinafter '836) in view of Rhim et al., USPN: 6,006,022 (hereinafter Rhim). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

Following are but a few examples as to how the certain claims from the instant invention and from the above patent are conflicting with each other.

As per instant claim 24, '836 claim 1 also recites (i) a set of instructions configured to including one or more user-defined addressing modes to reference data stored in memory; and (ii) a programmable address arithmetic unit with logic functions, i.e. the programmable portion, implementing said user-defined addressing modes to modify address in said memory held in registers, i.e. the fixed portion of the processor; said registers operatively coupled to said programmable AAU.

But '836 claim 1 does not explicitly specify a first program in a first programming program configured to implement user-defined address calculation; nor does '836 recite compiling a second program into object code having instructions comprising a fixed set of instructions that make use of a fixed set of addressing modes, wherein at least one instruction invokes the user-defined addressing mode. The memory with registers coupled with the

programmable AAU and having a set of instructions including one or more user-defined addressing modes as recited in (i) stands for the second program that make use of the user-defined addressing mode; and the programmable AAU as recited in (ii) to implement the user-defined addressing modes stands for the first program. The programmable AAU as in (ii) suggests that a program code in a programming language is to be written and compiled in order to fulfill what the user defines as addressing mode and computations; and the use of code instructions to implement register and memory data modification as a fixed portion of the computer program is further evidenced by Rhim. Rhim, in a method to use programming language to implement addressing mode analogous to '836 discloses first program (col. 7, lines 1-3; col. 14, lines 21-37; Figs. 11, 16) and second program (col. 12, lines 27-40) to implement user-defined functionalities or configuration and algorithm. In view of the teachings by Rhim, it would have been obvious for one of ordinary skill in the art to write a first program to implement the configuration or user-defined for the programmable AAU as in (ii) and to write a second program with instructions using registers with the fixed architecture of the computer as in (i) to make use of the addressing modes defined by the programmable AAU because programming languages are efficient means to implement functionalities that cannot be accomplished all by hardware; and using 2 programs for combining existing architecture of the host computer with programmable or configurable instructions would enhance the synergy of fixed architecture and programmable or user-defined capabilities as suggested by Rhim; and thereby make good use of resources at hand while maintaining a certain level of flexibility in configuring addressing modes.

As per instant claim 42, '836 claim 1 also recites a fixed set of instructions stored in memory refer to data of user-defined addressing modes; and a programmable AAU. But '836 claim 1 does not recites a first program to implement an algorithm on a processor; and a second program containing configuration data defining user-defined addressing mode; and executing said user-defined addressing mode by referencing an operand using said user-defined addressing mode. But in view of the teachings by Rhim and the rationale as set forth above, those limitations would also have been obvious.

As per claim 51, the rationale for obviousness as set forth in instant claim 24 above herein applies.

Likewise, **instant claims 60, 74, 77** can be matched against '836 claims 1, 8, 16, 17, 18, 21, 26, and 33 because these claims recite a fixed set of instructions in memory to perform arithmetic operations (ALU) connected to address program and configuration data from a user-defined addressing modes; and a programmable portion to implement said user-defined addressing modes. All these are combined with the rationale using Rhim as to render the features lacking in '836 obvious.

As per claims 69 and 77, '836 claims 19 and 27 have corresponding limitations because the latter claims also recite the auto-update features along with the limitations such as a fixed ALU unit and a separate PAAU, all of which combined with Rhim in order to apply the rationale for obviousness as set forth above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 33-34, 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhim et al., USPN: 6,006,022 (hereinafter Rhim), in view of Baxter, USPN: 6,182,206 (hereinafter Baxter).

As per claim 33, Rhim discloses:

supplying first software module comprising instructions from fixed set of instructions to implement an algorithm (e.g. *program residing in host 500, compile program 80 on host* -- col. 12, lines 27-40 – Note: analyzing memory activities and machine states is equivalent to control activities of interconnect unit and memory/address operations and the implementation of some algorithm, or control or diagnostic instructions);

supplying a second software module comprising configuration codes to define the operation of the user-defined address mapping function in the programmable interconnect circuitry (e.g. col. 7, lines 1-3; col. 14, lines 21-37; Figs. 11, 16 – Note: configuration via hardware definition language is user-defined), whereby

at least one instruction of said first module references an operand using such address mapping function in the interconnect circuitry (e.g. *load/store* – col. 10, line 60 col. 11, line 30 – Note: memory operations inherently include referencing of operands).

But Rhim fails to specify that the user-defined address mapping function is an user-defined addressing mode nor does Rhim specify implementing an algorithm using a processor having a programmable address arithmetic unit (PAAU).

Rhim mentions the use of simulation/verification with an analyzer to perform load/store transactions analysis, and cache miss exception detection, and register instruction debug logic (e.g. col. 10, line 47 to col. 11, line 58); as well as system address data exception detection (e.g. col. 15, lines 19-35); and suggests emulating a embedded target processor and detect arithmetic operation malfunctions therein (e.g. col. 1, lines 23-27; col. 2, lines 13-19); and programmable memory to dynamically accommodate real-time changes in the build logic and interconnect of such processors (col. 5, lines 36-44). One skilled in the art would recognize the suggestion by Rhim to emulate embedded processor in order to dynamically capture faults in memory related operations, thus prevent resources usage for recovery from memory erroneous referencing or cache misses, hence to alleviate/optimize processor resources. Further, Baxter, in a method to dynamically reconfigure memory organization microprocessor using PLA to address hardware operation logic and internal changes analogous to the method of configure and emulate hardware activities and/or system logic as taught by Rhim, discloses the a re-programmable address operate unit (*AOU*) to perform address-related operations coupled with the instruction fetched by the emulated processor (e.g. col. 7, line 60 to col. 8, line 21; col. 28, lines 17-51; Figs. 10-11). Baxter, like Rhim, also suggests the emulation to address the architecture specificity and performance optimization of embedded system processors, like DSP (e.g. col. 1, lines 30-48). Hence, in view of the suggestion by Rhim and teachings by Baxter, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement a programmable address arithmetic unit as suggested by Baxter to Rhim's method of debugging the memory-related operations and address/register operations as taught by Rhim. One would be motivated to do so because keeping track of the dynamic machine state of the execution while

emulating the hardware model in providing an programmable address arithmetic unit as claimed in order to addressing issues during processing the instructions (i.e. instructions of second program controlling the PAAU as claimed), and being able to reconfigure those addressing issues via such address arithmetic unit would alleviate subsequent memory faults in the iterative emulation process, and thereby optimizing the embedded microprocessor resources as have been suggested by Rhim and Baxter.

As per claim 34, Rhim suggests an embedded microprocessor (col. 1, lines 23-27) and Baxter discloses a emulating with HLL the operation of a DSP (col. 1, lines 30-48). One of ordinary skill in the art would have been motivated to apply the emulation of a embedded system as suggested by Rhim to an DSP as taught by Baxter, because DSP is handling computation-intensive or complex operations and that is exactly the reason for Rhim to emulate the operation of such complexity in order to capture dynamically the execution/exception state using an re-programmable interconnect system as disclosed, and thereby optimize its system resources utilization.

As per claim 38, in view of the combined teachings of Rhim and Baxter in claim 33 for the PAAU feature, this instant claim limitation would have been obvious because Rhim discloses configuring the PAAU blocks (e.g. PLA block *860* – Fig. 15) using the configuration code of said second program module.

As per claim 39, Rhim (with Baxter's teachings) only discloses sequence of input vectorized into sets, machine state snapshots, and register state observation per cycle (e.g. col. 11, lines 30-55; col. 12, lines 41-50; Fig. 5, 7) for emulation verification and testing but does not disclose micro-sequenced of state operations to implement the PAAU. Baxter discloses a

instruction sequencer to enable facilitate instruction execution as a state machine (e.g. Instruction state sequencer 100 – Fig. 5; col. 18, line 63 to col. 19, line 16; Fig. 6). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the state observation sequences as suggested in the memory vector/snapshot/register state debug and verification techniques by Rhim to include the instruction state sequencer, i.e. micro-sequenced state machine, as taught by Baxter because this would facilitate the observation at micro-level state of the instruction as it evolved into the PAAU configured by the HDL or second module, and thereby enabling the dynamic adjustment of the address resolution scheme intended in designing and optimizing the PAAU as suggested by the combination Baxter/Rhim.

As per claim 40, Rhim discloses a matrix for interconnecting the elements of the FPD or PLA and a latch and debugging logic (e.g. element 801a, Fig. 2; Fig. 14-17) but does not specify a cross-bar switching element. Baxter discloses a cross-bar switch while configuring the programmable data operating units (e.g. Fig. 8). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the interconnect circuitry by Rhim so to include a cross-bar switch to handle the selective routing of inputs going into the data handling units. In view of the disclosed latch and debugging logic and the interconnect circuit suggested by Rhim, and the teachings to use a cross-bar switch to route the correct data into the unit under emulation, it would have been obvious for one of ordinary skill in the art at the time the invention was made to include the cross-bar switch as taught by Baxter to Rhim's method to latch and debug modules interconnected by the second program in order to handle the PAAU circuitry emulation and debug as addressed in claim 33 because this cross-bar would impart the

selectivity of data entering the PAAU, thereby improve system debug error-preventing and efficiency.

As per claim 41, Rhim (combined with the PAAU teachings of Baxter) discloses dispatching subsets of instructions to functional units in a multi-use processor (col. 1, lines 13-60--Note: a microprocessor as suggested by Rhim is implicitly a multi-use processor), one of such functional units being the PAAU (e.g .col. 12, lines 20-62; Fig. 4).

7. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhim et al., USPN: 6,006,022, and Baxter, USPN: 6,182,206, as applied to claims 1, 33, 42, 51, 60, 69 above, and further in view of Stan Liao et al., "*Storage Assignment to Decrease Code Size*", June 1995, In Proceedings of ACM SIGPLAN'95, Conference on Programming Language Design and Implementation, Vol. 30, Issue 6, pp. 235—253 (hereinafter Liao).

As per claim 35, the combination Rhim/Baxter fails to disclose an instruction causing an auto-update, such auto-update operation being part of the addressing mode defined by the programmable system by the user. But Liao has disclosed the auto-update limitation as from above; and moreover, Liao discloses an operation with pointer operand that causes such auto-update operation (e.g. pg. 6, assembly code of Fig. 2 – Note: any indexed number is equivalent to a operand pointer causing an auto-increment/decrement, or offset assignment). It would have been obvious for one of ordinary skill in the art at the time the invention was made to enhance the address arithmetic unit as mentioned in the combined teachings/suggestions by Rhim/Baxter as in claim 33 above so to provide a functionality operable to perform with the arithmetic operations for auto-increment/decrement as taught by Liao, i.e. auto-update applying to operand pointer in addressing modes, because of the same reasons as set forth in claim 25 above.

As per claim 36, Liao also discloses assembly language mnemonic (see claim 35 – pg. 5, col. c -- Fig. 1).

As per claim 37, the combination Rhim fails to disclose an instruction used to specify one of the user-defined addressing modes to be selected to define the operation of auto-update. However, Baxter discloses a instruction set architecture or ISA instruction, i.e. the first module code as claimed, wherein is defined specific addressing modes (e.g. col. 12, lines 40-50) whereas Liao, in the high-level language or HLL-implemented algorithm to address instruction in a embedded architecture as mentioned in claim 25, discloses code generation step that selects addressing modes, i.e. *single indexing register with indirect auto-increment, and auto-decrement addressing modes* (pg. 3, first 3 paragraphs). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify Rhim's method to execute the configurable memory operations and code implemented circuitry thus disclosed so to include the addressing-mode-selecting code instruction as suggested by both Baxter and Liao, because this instruction to select the appropriate addressing mode in order to define which auto-update operation to implement would further enhance the architecture specificity as mentioned by Baxter, and thereby would alleviate resources usage for handling each addressing scenario given the limited register, storage and error handling capacities as known to be associated with the embedded systems like DSP as suggested by Baxter/Rhim and by Liao when Liao attempts to reduce the implementing code to cover the addressing operations.

Response to Arguments

8. Applicant's arguments with respect to claims 24-29, and 33-76 have been considered but some are moot in view of the current state of rejection.

The current rejection now addresses only claims 33-41, all of which are rejected under USC 35 103(a) and further falls under the ambit of USC 35 101 rejection.

(A) Applicants has submitted that Baxter teaches a reconfigurable architecture for use in programming of PLA but teaches away from the concept of coupling a fixed portion to a reconfigurable portion; and further teaches different instructions sets used per each different type of operation to be performed (Appl. Rmks. Pg. 13, 2nd and 3rd para). Examiner notes that claim 33 as recited, does not convey the concept that a fixed set of instructions is to be operable by being coupled with a programmable set of instructions in order to provide a useful result falling under the ambit of 'supplying software'. Hence the arguments questioning the reasons for Baxter to use the programmable set of instructions to achieve the addressing modes are moot because the invention as claimed does not provide the useful steps as to how to execute the method of supplying software. Nor does it make any connecting description relating the programmable portion and the fixed portion of software so as to enable the method of supplying software to be executed in order to yield a useful result within the computer art. The recited specifications as to further limit the software module being supplied are at best some intended use and do not bear any patentable weight over how the method of 'supplying software' is to be interpreted as useful invention. As long as the rejection provides some grounds to combine a programmable portion to a fixed architecture using a reasonable motivation, the rejection has fulfilled the method of supplying first and second software.

(B) Claims 42, 51, 60, 69 and 74 have been mentioned in Applicant's Remarks, but these arguments are moot in view of the newly established grounds of rejection.

Allowable Subject Matter

9. Claim 79 is allowed.

The following feature is allowable: processor comprising a programmable address arithmetic unit and a first software instructions comprising a fixed set of instructions to implement an algorithm and at least one user-defined auto-update addressing mode; a configuration data adapted to configure operation of at least one user-defined auto-update addressing mode in the PAAU, wherein op-code execution makes reference to an operand using the user-defined auto-update addressing mode instruction, by way of whose successive execution results in an addressing pattern, wherein the addressing pattern is non-linear and dependent on the application algorithm, and is using less cycles than would be possible by using a combination of instructions involving the fixed set of addressing modes.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

or: (703) 746-7240 (for informal or draft communications, please label

"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
January 12, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100